Amendment to the Claims

Kindly amend claim 1, cancel claims 8 & 9 without prejudice, and add new claims 34 & 35 as set forth below. In compliance with the Revised Amendment Format published in the Official Gazette on February 25, 2003, a complete listing of claims is provided herein. The changes in the amended claims are shown by strikethrough (for deleted matter) and underlining (for added matter).

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1. (Currently Amended) A structure comprising:

a first substrate and a second substrate; and

first solder bumps and second solder bumps offset therebetween, wherein said first solder bumps and said second solder bumps are separate solder bumps disposed between said first substrate and said second substrate, and wherein said second solder bumps have at least a portion that melts at a lower temperature than said first solder bumps; and

wherein said second solder bumps are for aligning said first substrate and said second substrate before melting said first solder bumps.

2. (Original) A structure as recited in claim 1, wherein said second solder bumps are larger than said first solder bumps.

3. (Original) A structure as recited in claim 1, wherein said second solder bumps comprise a portion having a higher concentration of tin than does said first solder bumps.

4. (Original) A structure as recited in claim 3, wherein said portion comprises a eutectic concentration of tin.

5. (Original) A structure as recited in claim 3, wherein said portion is adjacent to said second substrate.

6. (Original) A structure as recited in claim 3, wherein said portion is centrally located within said second solder bump.

7. (Original) A structure as recited in claim 3, wherein said portion is said entire second solder bumps.

8. (Canceled)

9. (Canceled)

10. (Original) A structure as recited in claim 1, wherein said second solder bumps melt at a temperature at least 25C less than said first solder bumps.

11. (Original) A structure as recited in claim 1, wherein said first substrate comprises a first semiconductor chip.

12. (Original) A structure as recited in claim 11, wherein said second substrate comprises a second semiconductor chip.

13. (Original) A structure as recited in claim 12, wherein said second chip is larger than said first chip.

14. (Original) A structure as recited in claim 12, wherein said second chip further comprises wire bond pads for bonding to a printed circuit board.

15-29. (Previously Canceled)

30. (Previously Added) A structure comprising:

a first substrate having a main surface with first solder bumps and second solder bumps separately disposed thereacross; and

wherein said second solder bumps have at least a portion that melts at a lower temperature than said first solder bumps, said second solder bumps being for aligning said first substrate to a second substrate before melting said first solder bumps.

31. (Previously Added) The structure of claim 30, wherein said second solder bumps are larger than said first solder bumps.

32. (Previously Added) The structure of claim 30, wherein said second solder bumps melt at a temperature at least 25°C less than said first solder bumps.

33. (Previously Added) The structure of claim 32, wherein the first substrate comprises a semiconductor chip.

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34. (New) The structure of claim 1, wherein said second solder bumps have a uniform composition and melt at a lower temperature than said first solder bumps.

35. (New) The structure of claim 30, wherein said second solder bumps have a uniform composition and melt at a lower temperature than said first solder bumps.